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APPLICATION

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TITLE: PREVENTING SILICIDE FORMATION AT THE GATE ELECTRODE IN A REPLACEMENT METAL GATE TECHNOLOGY

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PREVENTING SILICIDE FORMATION AT THE GATE ELECTRODE IN A REPLACEMENT METAL GATE TECHNOLOGY

Background

This invention relates generally to metal gate replacement technology.

In the fabrication of integrated circuits, it is sometimes desirable to selectively replace polysilicon gate structures with metal gate structures. To this end, some of the polysilicon gate structures may be removed and replaced with a metal gate structure.

Dual polysilicon gates are used in conventional complementary metal oxide semiconductor devices to engineer a desired low threshold voltage that is symmetric between NMOS and PMOS devices. Unfortunately, as the device's scale becomes smaller, this approach is not effective. When the polysilicon doping level is not sufficiently high, the polysilicon gate depletion effectively increases the gate dielectric thickness by several Angstroms. This negatively impacts the ability to scale gate dielectric thicknesses. Boron penetration and gate resistance may also be an issue for such polysilicon gate technology.

One approach to this problem is to replace the polysilicon gate with a metal gate. More, particularly, one metal gate may be utilized for the NMOS device and a different metal gate may be utilized for the PMOS device.

Thus, it may be desirable to form dual metal gate technology from conventional processing steps that use polysilicon. After the polysilicon has been defined to form the gate electrode for a transistor, the polysilicon may be removed. A different metal may be applied to form each of the NMOS and PMOS transistors.

In many polysilicon gate processes, a silicide is formed on the upper portion of the polysilicon gate. However, the formation of a silicide may make it very difficult to remove the polysilicon gate and to replace that polysilicon gate structure with a metal gate. In addition, the formation of etch byproduct residue may also block the polysilicon gate etch and removal sequence.

One solution to this problem is to overetch the silicide or etch byproduct residue. However, such overetching may result in adverse consequences to other materials. For example, the underlying gate oxide beneath the polysilicon gate may be etched due to the over extended polishing required for removal of the silicide or etch byproduct residue. Another solution is to use a nitride mask on top of the polysilicon to block silicide formation on the polysilicon while allowing silicide formation on the source/drain region.

Generally, a polysilicon opening polish process may result in excessive dishing in the field oxide areas before the nitride on the top of the polysilicon gates is removed.

If too much of the field oxide is lost, then the metal gate height is reduced and there may not be enough oxide left to reliably prevent the dishing in the damascene polish step from exposing the silicon surface.

Thus, there is a need for an improved technique for removing polysilicon gates as part of a metal gate replacement technology.

Brief Description of the Drawings

Figure 1 is a simplified, enlarged, partial cross-sectional view of one embodiment of the present invention at an early stage of manufacture;

Figure 2 is a simplified, enlarged, partial cross-sectional view of the embodiment shown in Figure 1 after further processing in accordance with one embodiment of the present invention;

Figure 3 is a simplified, enlarged, partial cross-sectional view of the embodiment shown in Figure 2 after subsequent processing in accordance with one embodiment of the present invention;

Figure 4 is a simplified, enlarged, partial cross-sectional view of another embodiment of the present invention; and

Figure 5 is a simplified, enlarged, partial cross-sectional view of the embodiment shown in Figure 4 further processing.

Detailed Description

Referring to Figure 1, a semiconductor wafer includes a substrate 10, such as a silicon substrate, that may be covered with a dielectric material 12 such as an oxide. Over the dielectric material 12 may be a patterned polysilicon gate structure 14 and a patterned polysilicon gate structure 14a.

Over the polysilicon gate structure 14 may be a mask 16 that, in one embodiment, may be a relatively thick nitride hard mask. The mask 16 is normally removed. However, in accordance with one embodiment of the present invention, the mask 16 is maintained over those transistor areas 20b (that will become replacement metal gate transistors) until the gate opening polish step in one embodiment of the present invention. The gate structure 14 in the areas 20b may be replaced with metal replacement.

A raised spacer 17 may be formed on sides of the polysilicon gate structure 14 to prevent silicide from forming at the edges. The spacer 17 may be formed of an insulator such as nitride or oxide.

Another polysilicon gate structure 14a in the area 20a may have its mask 16 removed and that gate structure 14a may have silicide formed on it. The gate structure 14a may be used for a polysilicon transistor.

In the gate opening polish step, an interlayer dielectric layer 19 may be polished down to the top of the mask 16 to enable the etch removal of the mask 16.

In one embodiment, a two-step polish process may involve a first stage using a hard pad to planarize and remove material in the vicinity of the tops of the mask 16 covered polysilicon gate structures 14. A second polish stage may utilize a soft pad and/or a slurry optimized to remove some or all of the mask material on top of the polysilicon gate structure 14.

The mask 16 may be etched away with a selective etch process to form the structure shown in Figure 2 after the silicidation processing has been completed in the areas 20a. A selective etch, such as H_3PO_4, may be used in some embodiments. In Figure 2, the polysilicon gate structure 14 is now exposed. The gate structure 14a is silicided in one embodiment of the present invention.

A selective etch of the polysilicon gate structure 14 is used to remove the polysilicon gate structure 14 from the dielectric 12. The removal of the polysilicon gate structure 14 may involve the use of a selective etch. Suitable selective etches include NH_4OH for NMOS gate structures 14 and tetramethylammonium hydroxide (TMAH) for PMOS gate structures 14. Since the gate structure 14 is substantially free of silicide it may ultimately be removed more easily.

Thereafter, a metal gate structure 18 may be deposited and patterned to achieve the structure shown in Figure 3. In accordance with some embodiments of the present invention, a polysilicon gate structure 14 to be replaced may be protected from silicidation. In addition, in some embodiments, a high quality etch may be utilized. Also, the dielectric lost during polishing may be reduced in some embodiments.

In some embodiments, improved etch reliability and improved dielectric maintenance may be achieved. These results may, in some embodiments, enable better margins in the later metal gate damascene polishing steps.

In another embodiment of the present invention, a mask etch stop layer may be located above the mask 16 at the point shown in Figure 1. In this case, the polish may stop after exposing the etch stop layer and a mask etch may be used to remove the etch stop layer and the mask 16.

In still another embodiment of the present invention, a slurry may be used that has a higher mask 16 polish removal rate than the dielectric 12 removal rate. This combines the functionality of the mask etch with the polish and may reduce or eliminate the mask etch part of the process shown in Figures 1 through 3.

In one embodiment, the polishing of the structure may only expose the top of the mask 16. This exposes the

dielectric material 12 to a reduced over-polishing relative to other techniques.

Referring to Figure 5 in accordance to another embodiment of the present invention, a nitride layer 22 may be formed over the gate structure 14 and mask 16. An interlayer dielectric 19 may overlie the lower portions of the nitride layer 22. Some of the overlying interlayer dielectric material 19 may be polished away to achieve the structure shown in Figure 4. Thereafter, an etching process may remove the exposed nitride layer 22 and the mask 16.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: